AMENDMENTS TO THE CLAIMS

1. (Previously presented) A method of operating a sense amplifier to read data stored in a memory cell, the method comprising steps of:

pre-charging a bit-line of the memory cell to a predetermined reference voltage substantially equal to a trip point of the sense amplifier using a pre-charging circuit;

developing a voltage signal representing data stored in the memory cell;

reconfiguring the pre-charge circuit as a regeneration circuit; and

amplifying the voltage signal using the regeneration circuit such that the amplified voltage signal increasingly deviates from the predetermined reference voltage with increasing time.

2. (Original) A method according to claim 1, further including the step of pre-charging a node of a cascode device coupled to the bit-line of the memory cell.

3. (Cancelled)

4. (Cancelled)

5. (Currently amended) A sense amplifier to read a multi-state memory cell having a field effect transistor (FET) with a source, a drain and a bit-line, the sense amplifier comprising:

a device coupled to the drain of the FET of the memory cell, the device adapted to increase the resolution of the sense amplifier during a read mode and to isolate the sense amplifier from a high voltage applied to the memory cell during a write mode; and

a pre-charge circuit coupled to a device, the pre-charge circuit configured to pre-charge the bit-line of the memory cell through ~~the~~ a cascode device during a pre-charge mode to reduce time required to read the multi-state memory cell,

wherein the pre-charge circuit comprises a unity gain buffer having an input to which a predetermined reference voltage is applied, and an output coupled to provide a bias current (I_{BIAS}) to the cascode device to ~~pre-chare~~ pre-charge the bit-line by charging a node of the cascode device to the predetermined reference voltage.

6. (Original) A sense amplifier according to claim 5, wherein the pre-charge circuit further comprises a transistor switch to couple the unity gain buffer to the cascode device during

the pre-charge mode and to de-couple the unity gain buffer from the cascode device during a develop mode.

7. (Currently amended) A sense amplifier according to claim 6, further comprising a reference current circuit to provide a reference current (I_{REF}), wherein in the develop mode a difference between I_{REF} and a current through the memory cell (I_{CELL}) causes a change from the predetermined reference voltage to which the node of the cascode device is charged to develop a voltage signal representing data stored in the memory cell.

8. (Original) A sense amplifier according to claim 7, wherein the pre-charge circuit is re-configurable as a regeneration circuit during a regeneration mode to amplify the voltage signal developed during the develop mode.

9. (Cancelled)

10. (Currently amended) In a memory having at least one multi-state memory cell capable of storing data therein and a sense amplifier capable of reading data stored in the memory cell, the sense amplifier having a cascode device ~~doubled~~ coupled to the memory cell and a pre-charge circuit for pre-charging a bit-line of the memory cell through the cascode device, a method of operating the memory to read data stored in the multi-state memory cell, the method comprising the steps of:

coupling the pre-charge circuit to the cascode device;

pre-charging the bit-line of the memory cell through the cascode device to a predetermined reference voltage;

de-coupling the pre-charge circuit from the cascode device;

developing a voltage signal representing data stored in the memory cell;

reconfiguring the pre-charge circuit as a regeneration circuit; and

amplifying the voltage signal using the regeneration circuit such that the amplified voltage signal increasingly deviates from the predetermined reference voltage with increasing time.

11. (Original) A method according to claim 10, herein the pre-charge circuit comprises a unity gain buffer having a output switchably coupled to the cascode device, and

wherein the step of coupling the pre-charge circuit to the cascode device includes applying a control signal to couple the output to the cascode device.

12. (Currently amended) A method according to claim 11, wherein the step of pre-charging the cascode device to a predetermined reference voltage includes:

applying the predetermined reference voltage to an input ~~to~~ of the unity gain buffer; and

applying a bias current (I_{BIAS}) from the unity gain buffer to the cascode device to pre-charge the bit-line of the memory cell by charging the node of the cascode device to the predetermined reference voltage.

13. (Original) A method according to claim 12, wherein the sense amplifier further comprises a reference current circuit to provide a reference current (I_{REF}) to the cascode device, and wherein the step of pre-charging the cascode device to a predetermined reference voltage includes applying I_{REF} and I_{BIAS} simultaneously to the cascode device to pre-charge the bit line through the cascode device to the predetermined reference voltage.

14. (Original) A method according to claim 13, wherein the step of developing a voltage signal includes enabling a difference between I_{REF} and a current through the memory cell (I_{CELL}) to cause a change from the predetermined reference voltage to which the cascode device is charged.

15. (Original) A method according to claim 10, wherein the step of reconfiguring the pre-charge circuit as a regeneration circuit includes forming an amplifier having a positive feedback loop.

16. (Original) A method according to claim15, wherein the pre-charge circuit comprises a unity gain buffer, and wherein forming an amplifier includes forming the amplifier using components comprising the unity gain amplifier.

17. (Original) A method according to claim 15, wherein the step of amplifying the voltage signal includes amplifying the voltage signal using the amplifier.

18. (Previously presented) A multi-state memory comprising:

at least one multi-state memory cell capable of storing data therein;

a sense amplifier capable of reading data stored in the memory cell, the sense amplifier including:

a cascode device coupled to the memory cell;

a pre-charging circuit for pre-charging a bit-line of the at least one multi-state memory cell through the cascode device;

a developing circuit for developing a voltage signal representing data stored in the memory cell using a reference current; and

an amplifying circuit for amplifying the voltage signal such that the amplified voltage signal increasingly deviates from the predetermined reference voltage with increasing time.

19. (Previously presented) A multi-state memory comprising:

at least one multi-state memory cell capable of storing data therein;

a sense amplifier capable of reading data stored in the memory cell, the sense amplifier including:

a cascode device coupled to the memory cell;

a pre-charging circuit for pre-charging a bit-line of the at least one multi-state memory cell through the cascode device;

a developing circuit for developing a voltage signal representing data stored in the memory cell using a reference current; and

an amplifying circuit for amplifying the voltage signal,

wherein the pre-charging circuit comprises a unity gain buffer having an input to which a predetermined reference voltage is applied, and an output coupled to provide a bias current (I_{BIAS}) to the cascode device to pre-charge the bit-line by charging the node of the cascode device to the predetermined reference voltage.

20. (Currently amended) A multi-state memory according to claim 19, wherein the developing circuit comprises:

means for decoupling the output of the pre-charge circuit from the cascode device; ~~and~~

a reference current circuit to provide a reference current (I_{REF}) to the cascode device; and

wherein a difference between I_{REF} and a current through the memory cell (I_{CELL}) causes a change from the predetermined reference voltage to which the node of the cascode device is charged.

21. (Currently amended) A multi-state memory according to claim 19, wherein the ~~means~~ developing circuit for developing a voltage signal ~~developing circuit~~ comprises a regeneration circuit having an amplifier with a positive feedback loop.

22. (Original) A multi-state memory according to claim 21, wherein the pre-charging circuit comprises components of the unity gain amplifier coupled together in a first configuration, and wherein the regeneration circuit comprises components of the unity gain amplifier coupled together in a second configuration.